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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/973,888	10/11/2001	Kazuhiro Okabayashi	60188-108	8960

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EXAMINER	
YANCHUS III, PAUL B	

ART UNIT	PAPER NUMBER
2116	

DATE MAILED: 06/10/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/973,888	OKABAYASHI ET AL.	
	Examiner	Art Unit	
	Paul B Yanchus	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claim 1 is rejected under 35 U.S.C. 102(b) as being anticipated by Yamauchi et al., US Patent no. 5,903,503 [Yamauchi].

Yamauchi teaches an integrated circuit having a multiprocessor architecture, the circuit comprising:

a first processor [EU1 in Figure 13 and column 33, line 10], which operates synchronously with a first internal clock signal [CK1 in Figure 13];

a second processor [EU2 in Figure 13 and column 33, line 11], which operates synchronously with a second internal clock signal [CK1 in Figure 13];

a memory [RAM in Figure 13], which operates synchronously with a third internal clock signal [CK1 in Figure 13] ; and

a clock supply unit [SUB CLOCK GENERATOR1 in Figure 13], which generates, from an external clock signal [CK0 in Figure 13], three clock signals that are in phase with each other, and which supplies the clock signals as the first, second and third internal clock signals, respectively [CK1 being supplied to EU1, EU2 and RAM in Figure 13] ;

wherein the first processor, the second processor, the memory, and the clock supply unit are integrated together on a single chip [LSI chip, column 33, line 10 and Figure 13].

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamauchi et al., US Patent no. 5,903,503 [Yamauchi], in view of Applicant's Admitted Prior Art [AAPA].

Yamauchi teaches an integrated circuit having a multiprocessor architecture with shared memory, but does not explicitly teach the specific components of the memory and their operations.

AAPA teaches a well known multiprocessor architecture with shared memory. Specifically, AAPA teaches that it is well known in the art for a memory to comprise:

a memory array which is used to store data [MEMORY in Figure 10], and

a memory controller interposed between the first processor [element 500 in Figure 10] and the memory array [MEMORY in Figure 10] and between the second processor [element 510 in Figure 10] and the memory array,

wherein the memory controller, receives a first memory access signal [MRW1 in Figure 10], a first address [ADRS1 in Figure 10], a second memory access signal [MRW2 in Figure 10] and a second address [ADRS2 in Figure 10], the first memory access signal and the first address being output by the first processor [element 500 in Figure 10], the second memory

access signal and the second address being output by the second processor [element 510 in Figure 10];

selects and provides the first address to the memory array when the first memory access signal is asserted [page 3, line 19 – page 4, line 5; and

selects and provides the second address to the memory array when the second memory access signal is asserted [page 4, lines 6-12].

It would have been obvious to one of ordinary skill in the art to include the well known memory structure taught by AAPA into the integrated circuit taught by Yamauchi to manage read and write requests from the plurality of processors.

Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamauchi et al., US Patent no. 5,903,503 [Yamauchi], in view of Cai et al., US patent no. 6,631,474 [Cai].

Yamauchi teaches an integrated circuit having a multiprocessor architecture, but does not explicitly teach receiving a plurality of terminating signals and supplying clock signals clock signals to system components based on the state of the terminating signals.

Cai teaches a multiprocessor system in which a control circuit [ICL, column 4, lines 40-43]:

receives a first terminating signal [signal indicating that system is plugged in] and a second terminating signal [signal indicating that system is operating on battery power, column 5, lines 60-65];

disables a first processor [low-power processor] when the first terminating signal is solely asserted [system is plugged in, column 6, lines 10-15]; and

disables a second processor [high-power processor] when the second terminating signal is solely asserted [system is operating on battery power, column 5, line 64 – column 6, line 5].

It would have been obvious to one of ordinary skill in the art to selectively operate each of the processors in the system taught by Yamauchi to reduce the power consumption of the system and consequently enable the system to operate for longer periods of time when available power is limited.

Cai does not explicitly teach disabling the processors by stopping the supply of clock signals to the processors. However, it is well known in the art that stopping the supply of a clock to a clocked device will disable the device and consequently reduce power consumption of the device. It would have been obvious to one of ordinary skill in the art to disable the processors taught by Cai by stopping the corresponding clock supplies in order to reduce power consumption of the system.

Cai also does not explicitly teach disabling the system memory when the two processors are disabled. However it would have been obvious to one of ordinary skill in the art to disable the system memory when the two processors are disabled since the system memory would not be accessed. Disabling the system memory when it is not needed would further reduce power consumption of the system.

Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamauchi et al., US Patent no. 5,903,503 [Yamauchi], in view of Terashima, US Patent no. 6,289,436.

Yamauchi teaches an integrated circuit having a multiprocessor architecture, but does not explicitly teach reset control unit for receiving external reset signals and generating internal reset signals for resetting system components.

Terashima teaches a reset control unit for receiving external reset request signals and selectively generating internal reset commands to the system components based on the external reset request signals and the system state [column 5, line 65 – column 6, line 62].

It would have been obvious to one of ordinary skill in the art to utilize the reset circuitry taught by Terashima with the system taught by Yamauchi in order to ensure that the proper internal components are reset in response to external reset requests.

Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamauchi et al., US Patent no. 5,903,503 [Yamauchi] and Terashima, US Patent no. 6,289,436, in view of Cai et al., US patent no. 6,631,474 [Cai].

Yamauchi and Terashima teach an integrated circuit having a multiprocessor architecture, but do not explicitly teach receiving a plurality of terminating signals and supplying clock signals clock signals to system components based on the state of the terminating signals.

Cai teaches a multiprocessor system in which a control circuit [ICL, column 4, lines 40-43]:

receives a first terminating signal [signal indicating that system is plugged in] and a second terminating signal [signal indicating that system is operating on battery power, column 5, lines 60-65];

disables a first processor [low-power processor] when the first terminating signal is solely asserted [system is plugged in, column 6, lines 10-15]; and

disables a second processor [high-power processor] when the second terminating signal is solely asserted [system is operating on battery power, column 5, line 64 – column 6, line 5].

It would have been obvious to one of ordinary skill in the art to selectively operate each of the processors in the system taught by Yamauchi and Terashima to reduce the power consumption of the system and consequently enable the system to operate for longer periods of time when available power is limited.

Cai does not explicitly teach disabling the processors by stopping the supply of clock signals to the processors. However, it is well known in the art that stopping the supply of a clock to a clocked device will disable the device and consequently reduce power consumption of the device. It would have been obvious to one of ordinary skill in the art to disable the processors taught by Cai by stopping the corresponding clock supplies in order to reduce power consumption of the system.

Cai also does not explicitly teach disabling the system memory when the two processors are disabled. However it would have been obvious to one of ordinary skill in the art to disable the system memory when the two processors are disabled since the system memory would not be accessed. Disabling the system memory when it is not needed would further reduce power consumption of the system.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Young, US Patent no. 5,991,819 teaches a multiple processor system with shared system memory.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul B Yanchus whose telephone number is (703) 305-8022. The examiner can normally be reached on Mon-Thurs 8:00-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne H Browne can be reached on (703) 308-1159. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Paul Yanchus
June 2, 2004

THOMAS LEE
SUPERVISORY PATENT EXAMINER
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